Midterm Exam

(February 15th @ 5:30 pm)

Presentation and clarity are very important! Show your procedure!

Problem 1 (20 pts)

a) Complete the following table. The decimal numbers are unsigned: (5 pts.)

Decimal	BCD	Binary	Reflective Gray Code
			101010
		1100010	
	010101110110		

b) Complete the following table. Use the fewest number of bits in each case: (12 pts.)

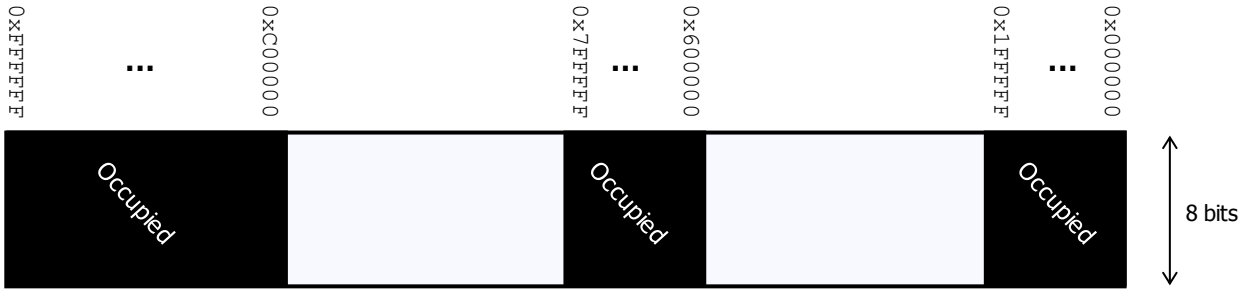
REPRESENTATION			
Decimal	**Sign-and-magnitude**	**1's complement**	**2's complement**
	1100110		
		11111	
			100000
		01000101	
-64			
			101000

c) Convert the following decimal numbers to their 2's complement representations. (3 pts.)

- ✓ -16.3125
- ✓ 18.375

Problem 2 (11 pts)

- The figure below depicts the entire memory space of a microprocessor. Each memory address occupies one byte. 1KB = 2^{10} bytes, 1MB = 2^{20} bytes, 1GB = 2^{30} bytes
  - ✓ What is the size (in bytes, KB, or MB) of the memory space? What is the address bus size of the microprocessor? (2 pts.)
  - ✓ If we have a memory chip of 2 MB, how many bits do we require to address those 2 MB of memory? (1 pt.)
  - ✓ We want to connect the 2 MB memory chip to the microprocessor. For optimal implementation, we must place those 2 MB in an address range where every single address shares some MSBs. Provide a list of all the possible address ranges that the 2 MB chip can occupy. You can only use the non-occupied portions of the memory space as shown below.



Problem 3 (10 pts)

- Given two 4-bit signed (2's complement) numbers A, B, sketch the circuit that computes $(A - B) \times 3$. You can only use adder units (or full adders if you prefer) and logic gates. Make sure your circuit avoids overflow.

Problem 4 (17 pts)

a) Perform the following additions and subtractions of the following unsigned integers. Use the fewest number of bits n to represent both operators. Indicate every carry (or borrow) from c_0 to c_n (or b_0 to b_n). For the addition, determine whether there is an overflow. For the subtraction, determine whether we need to keep borrowing from a higher byte. (6 pts.)

- ✓ 29 - 51
- ✓ 41 + 37

b) Perform the following operations, where numbers are represented in 2's complement. Indicate every carry from c_0 to c_n. For each case, use the fewest number of bits to represent the summands and the result so that overflow is avoided. (8 pts.)

- ✓ 62 - 79
- ✓ -53 - 26

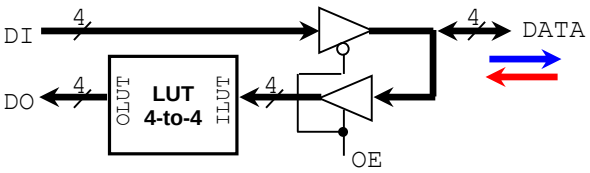
c) Get the multiplication result of the following numbers that are represented in 2's complement arithmetic with 4 bits. (3 pts.)

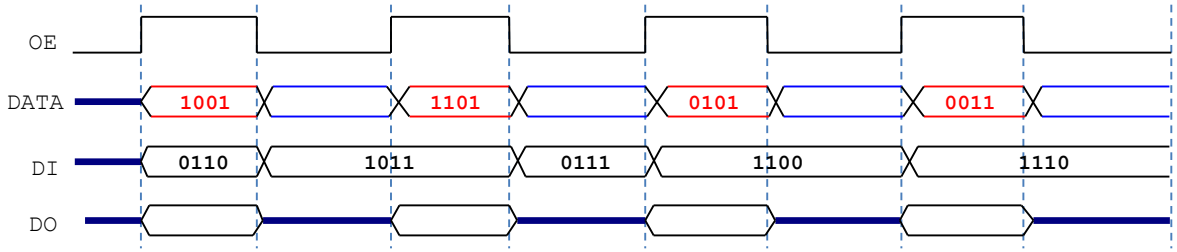
- ✓ -5 x 7

PROBLEM 5 (10 PTS)

- Given the following circuit, complete the timing diagram (signals DO and $DATA$).
  The LUT 4-to-4 implements the following function: $OLUT = [sqrt(ILUT)]$. For example: $ILUT = 1100 \rightarrow OLUT = 0100$

Input data to LUT is treated as an unsigned number.



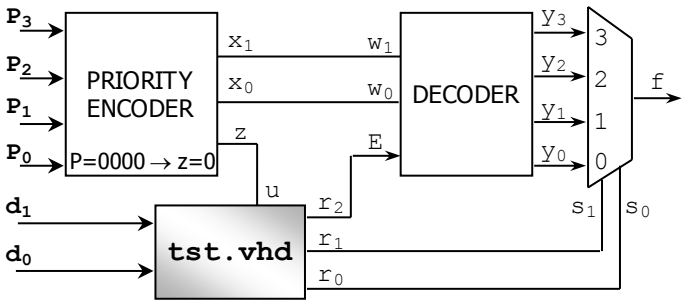


PROBLEM 6 (17 PTS)

- Sketch the circuit that implements the following Boolean function: $f = a \oplus b \oplus c \oplus d$
  Recall that $a \oplus b \oplus c \oplus d = (a \oplus b) \oplus (c \oplus d)$
  - ✓ Using ONLY an 8-to-1 MUX and NOT gates. (3 pts.)
  - ✓ Implement the previous circuit using ONLY 2-to-1 MUXs (AND, OR, NOT, XOR gates are not allowed). (14 pts.)

PROBLEM 7 (15 PTS)

- Complete the timing diagram of the following circuit. The VHDL code (`tst.vhd`) corresponds to the shaded circuit.
  $d = d_1 d_0$, $w = w_1 w_0$, $r = r_2 r_1 r_0$, $y = y_3 y_2 y_1 y_0$




```
library ieee;
use ieee.std_logic_1164.all;
entity tst is
  port (d: in std_logic_vector(1 downto 0);
        r: out std_logic_vector(2 downto 0);
        u: in std_logic);
end tst;
```

```
architecture bhv of tst is

begin

  process (d, u)
  begin

     r <= d&'0';
     if u = '1' then
        r <= '1'&d;
     end if;

  end process;

end bhv;
```